

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,716,714 B1
DATED : April 6, 2004
INVENTOR(S) : Herbert Goebel et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page.

Item [57], ABSTRACT,

Line 8, change "voltage of diode." to -- voltage of the diode --

Column 1.

Line 33, change "the silicon" to --the silicon chip, the allowable

current load to be increased and the thermal loading of the silicon chip to be reduced in a manner that can be realized relatively simply. In so doing, a reduction in the forward voltage is simultaneously achieved. The effect of additional saw grooves is particularly advantageous, because later, when the socket and lead wire are soldered to the diode chip, the grooves lead to a better, bubble-free soldering procedure (capillary effect), and the grooves filled with solder result in additional, more effective cooling of the chip, which extends into the depth of the silicon body and therefore thermally couples the chip to the heat sink in a more effective manner.

BRIEF DESCRIPTION OF THE DRAWINGS, should read as follows:

Fig. 1a shows a cross-sectional side view of a diode in accordance with the present invention.

Fig. 1b shows a plan view of the diode shown in Fig. 1a.

Fig. 2 shows a semiconductor wafer used as the starting material in a method for producing the semiconductor arrangement in accordance with the present invention.

Fig. 3 shows the semiconductor wafer in a further method step for producing the semiconductor arrangement in accordance with the present invention.

Fig. 4 shows the semiconductor wafer in yet another method step for producing the semiconductor arrangement in accordance with the present invention.--

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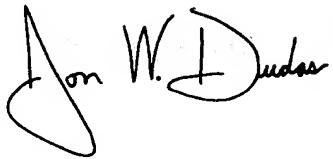
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2.

Line 43, change "neutral is filing" to -- neutral filing --

Signed and Sealed this

Fourteenth Day of June, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office